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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,787	SETHI ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 03/12/2007 have been fully considered but they are not persuasive. Objection to Figure 3 is withdrawn. Rejection of claims 3-4, 8, 10, 13, 16 and 20 under 35 U.S.C. 112 second paragraph are withdrawn. Rejection of claims 1-11 and 18-21 under 35 U.S.C. 101 are withdrawn. Currently, claims 1-21 are pending for examination.

2. In response to applicant's arguments, on page 7, 4th paragraph, regarding amended independent claim 1 rejected under 35 U.S.C. 102(a) that the Guide (i.e. "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors") does not teach/suggest decoding a memory configuration access within a decoder of a processor to configure an integrated device in another processor; applicant's arguments have fully been considered, but are not found to be persuasive.

The Guide teaches decoding (i.e. decoding by initialization) a memory configuration access within a decoder of a second processor (e.g. bootstrap processor (BSP)) to configuring an integrated device (e.g. memory controller) in a first processor (e.g. processor node or application processor (AP)) (pages 21-23), as the BSP (e.g. second processor with decoder) is responsible for the configuring and initialization (e.g. decoding) of the memory controller (e.g. integrated device) on all processor nodes (e.g. first processor), enabling the

processor nodes to shift from not accessible (e.g. unconfigured state) to accessible (e.g. configured state).

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 4, 6, 9-10, 12-13, 15-16, 18 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors".

6. As per claim 1, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device (e.g. memory controller) in a first processor (e.g. processor node or

application processor (AP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23) comprising:

decoding (decoding by initialization) a memory configuration access within a decoder of a second processor (e.g. bootstrap processor (BSP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23), wherein the BSP inherently include the decoder in order to implementing the decoding,

the second processor coupled to the first processor, to a configuration cycle (Section 3.1 on page 25);

routing the configuration cycle to a chipset (e.g. host bridge) based at least in part on a routing information (Section 2.1.1 on pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203); and

forwarding the configuration cycle to configure the integrated device from an unconfigured state (e.g. not accessible) to a configured state (e.g. accessible) (page 21 and Section 2.1.4 on page 23).

7. As per claim 4, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the method comprising wherein the chipset has a bridge (e.g. host bridge) and adheres to an interconnection that is in accordance with a predetermined protocol (e.g. PCI protocol) (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25).

8. As per claim 6, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated

device (e.g. circuitry utilized for the address map table) in a first processor (e.g. processor node or application processor (AP)) (Section 2.1 on page 21 and Section 2.1.5 on page 23) comprising:

decoding (decoding by initialization) an Input Output (IO) configuration access within a second processor (e.g. bootstrap processor (BSP)), coupled to a first processor, to a configuration cycle (Section 2.1 on page 21 and Section 2.1.5 on page 23); and

routing the configuration cycle to the integrated device (e.g. memory controller) based at least in part on a routing information to configure the integrated device (e.g. memory controller) from an unconfigured state (e.g. not accessible) to a configured state (e.g. accessible) (pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203).

9. As per claim 9, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the method comprising wherein the configuration adheres to an interconnection of predetermined protocol (e.g. PCI protocol) (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25).

10. As per claim 10, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the method comprising wherein the predetermined protocol comprises a PCI type interconnect protocol (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25).

11. As per claims 12, 15 and 18, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a system and an article of manufacture comprising a machine readable medium comprising:

a first processor (e.g. bootstrap processor (BSP)) with a decoder coupled to a second network component (e.g. processor node or application processor (AP)) with an integrated device (Section 2.1 on pages 21 and Section 3.1 on page 25), wherein BSP is responsible for the initialization process, therefore must have the necessary decoder to implement the initialization process;

the decoder to decode (decode by initiation) either a memory or IO configuration access to a configuration cycle (Section 2.1 on page 21; Section 2.1.4-2.1.5 on page 23 and Section 3.1 on page 25); and

to transmit (transmit by routing) the configuration cycle to either a chipset (e.g. host bridge) or the integrated device, wherein the configuration cycle adheres to a first type of interconnect protocol (e.g. PCI protocol) (Section 2.1.1 on pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203).

12. As per claim 13, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the processor comprising wherein the transmission of the configuration to either the chip set or integrated device is via a PCI type interconnection (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25).

13. As per claim 16, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the system comprising wherein the first type of interconnection protocol comprises a PCI type protocol (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25).

14. As per claim 20, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches the article of manufacture comprising wherein the first type of interconnect protocol is in accordance with a PCI type protocol (Section 2.1.1 on pages 21-22 and Section 3.1 on page 25)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2-3, 5, 7-8, 11, 14, 17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors" in view of "HyperTransport™ Technology I/O Link".

16. As per claims 2-3, 5, 7-8, 11, 14, 17 and 19, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches all the

limitations of claim 1 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the method comprising the utilization of HyperTransport Links (Section 2.1.1 on page 21-22); the configuration cycle is routed to the chipset (e.g. host bridge) (Section 3.1 on page 25); and wherein the chipset or integrated device (e.g. memory controller) is coupled to a decoder (e.g. decoder utilized for initialization) of a first processor (e.g. bootstrap processor (BSP)) (Section 2.1 on pages 21 and Section 3.1 on page 25).

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors does not expressly teaches the method comprising:

wherein the configuration cycle is to be routed to the chipset via a network fabric;

wherein the network fabric is a plurality of point to point links;

wherein the second processor is coupled to the first processor via the network fabric; and

wherein the chipset or the integrated device is coupled to the decoder via a network fabric.

HyperTransport™ Technology I/O Link teaches the system and method comprising a networking of a plurality of processor (Fig. 10 on page 20), wherein the networking comprises a point-to-point link ("The HyperTransport™ Technology Solution" Section on page 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include HyperTransport™ Technology I/O Link's

networking and point-to-point link into BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' method in order to conform to the standard set forth by the HyperTransport™ I/O Link Specification as BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors utilized the plurality of HyperTransport links. The resulting combination of the references teaches the method further comprising:

wherein the configuration cycle is routed to the chipset through the network interconnection;

wherein the network interconnection comprises the plurality of point-to-point links;

wherein the second processor is coupled to the first processor through the network interconnection; and

wherein the host bridge is coupled to the decoder via the network interconnection.

17. As per claim 21, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device (e.g. memory controller) in a first processor (e.g. processor node or application processor (AP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23) comprising:

decoding (decoding by initialization) a memory configuration access within a second processor (e.g. bootstrap processor (BSP)) (Section 2.1 on page 21 and Section 2.1.4 on page 23),

the second processor coupled to the first processor, to a configuration cycle (Section 3.1 on page 25); and

routing the configuration cycle from the second processor (E.g. BSP) to the first processor (e.g. processor nodes or AP) to configure the integrated device from an unconfigured state (e.g. not accessible) to a configure state (e.g. accessible) (pages 21-22; Section 3.1 on page 25 and Chapter 8 on page 203).

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors does not expressly teach the method comprising wherein routing the configuration cycle from a chipset to the first processor via a bridge.

HyperTransport™ Technology I/O Link teaches the system and method comprising a multiple chain of tunnel devices connected to a bridge, which is then connected to a host bridge ("Device Configuration" section on page 7).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include HyperTransport™ Technology I/O Link's interconnection utilizing the host bridge and bridge into BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' method in order to conform to the standard set forth by the HyperTransport™ I/O Link Specification as BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors utilized the plurality of HyperTransport links. The resulting combination of the references teaches the method further comprising the routing of the configuration cycle from the host bridge (chipset) to the bridge then to the first processor.

IV. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-21 have received a final action on the merits. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 27, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER